

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A data writing method for a semiconductor memory device having a first memory cell block capable of rewriting data and having at least one first memory cell; and a second memory cell block capable of rewriting data and having at least one second memory cell adjoining said first memory cell, said method comprising:

writing data into said first memory cell;

writing data into said second memory cell following writing the data into said first memory cell;

verifying the data of said first memory cell after writing the data into said second memory cell; and

rewriting the data into said first memory cell when insufficiency of the data of said first memory cell as a result of verifying the data of said first memory cell.

Claim 2 (Original): The method according to claim 1, wherein said first and second memory cells have a charge accumulation layer, respectively, in which the electric charge is injected or discharged in association with the data to be stored and store the data of 2 values or more as an electric charge amount.

Claim 3 (Original): The method according to claim 1, wherein said first and second memory cells have a charge accumulation layer, respectively, in which the electric charge is injected or discharged in association with the data to be stored, store the data of 2 values or more as an electric charge amount and store the data of 3 values or more supplied from the outside in association with the data of 2 values of each of said first and second memory cells.

Claim 4 (Original): A data writing method for a semiconductor memory device having a memory cell block capable of rewriting data, wherein said memory cell block has at least two first and second memory cells connected in series or in parallel and adjoin each other, said method comprising:

writing data into said first memory cell;

writing data into said second memory cell following writing the data into said first memory cell;

verifying the data of said first memory cell after writing the data into said second memory cell; and

rewriting the data into said first memory cell when insufficiency of the data of said first memory cell as a result of verifying the data of said first memory cell.

Claim 5 (Original): The method according to claim 4, wherein said first and second memory cells have a charge accumulation layer, respectively, in which the electric charge is injected or discharged in association with the data to be stored and store the data of 2 values or more as an electric charge amount.

Claim 6 (Original): The method according to claim 4, wherein said first and second memory cells have a charge accumulation layer, respectively, in which the electric charge is injected or discharged in association with the data to be stored, store the data of 2 values or more as an electric charge amount and store the data of 3 values or more supplied from the outside in association with the data of 2 values of each of said first and second memory cells.

Claims 7-61 (Canceled).

Claim 62 (New): The method according to claim 1, wherein each of said first and second memory cells comprises an field effect transistor having at least one charge accumulation layer and at least one control gate.

Claim 63 (New): The method according to claim 62, wherein said field effect transistors are formed on the same conductive type well, respectively.

Claim 64 (New): The method according to claim 62, wherein said field effect transistors use an FN tunneling current for the writing operation.

Claim 65 (New): The method according to claim 62, wherein each of said first and second memory cells includes at least first and second cell transistors adjoining each other, each of said first and second cell transistor have a source electrode, a drain electrode and said charge accumulation layer, said source electrode of said first cell transistor and said drain electrode of said second cell transistor are connected in series with each other, and a distance between said charge accumulation layer of said first cell transistor and said charge accumulation layer of said second cell transistor is less than twice a thickness of said charge accumulation layer.

Claim 66 (New): The method according to claim 65, wherein an insulator is formed between the charge accumulation layer of said first memory cell and the charge accumulation layer of said second memory cell.

Claim 67 (New): The method according to claim 62, wherein said charge accumulation layer comprises an insulator.

Claim 68 (New): The method according to claim 4, wherein each of said first and second memory cells comprises an field effect transistor having at least one charge accumulation layer and at least one control gate.

Claim 69 (New): The method according to claim 68, wherein said field effect transistors are formed on the same conductive type well, respectively.

Claim 70 (New): The method according to claim 68, wherein said field effect transistors use an FN tunneling current for the writing operation.

Claim 71 (New): The method according to claim 68, wherein each of said first and second memory cells includes at least first and second cell transistors adjoining each other, each of said first and second cell transistor have a source electrode, a drain electrode and said charge accumulation layer, said source electrode of said first cell transistor and said drain electrode of said second cell transistor are connected in series with each other, and distance between said charge accumulation layer of said first cell transistor and said charge accumulation layer of said second cell transistor is less than twice a thickness of said charge accumulation layer.

Claim 72 (New): The method according to claim 71, wherein an insulator is formed between the charge accumulation layer of said first memory cell and the charge accumulation layer of said second memory cell.

Claim 73 (New): The method according to claim 68, wherein said charge accumulation layer comprises an insulator.